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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/084,566	02/27/2002	Philip E. Madrid	5500-80100 TT 4987	7963

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EXAMINER	
PATEL, NITIN C	
ART UNIT	**PAPER NUMBER**
2116	

DATE MAILED: 05/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/084,566	MADRID ET AL.	
	Examiner	Art Unit	
	Nitin C. Patel	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 April 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) *5* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4 and 6-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 June 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This is in responsive to amendment filed on 25 April 2005.

2. Claim 5 has been cancelled.

3. Claims 1 – 4, and 6 – 26 are presented for the examination.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. Claims 1 – 4, and 6 – 26, are rejected under 35 U.S.C. 103(a) as being unpatentable over Thor, US Patent 5,964,881, and further in view of Yenisey, US Patent 4,471,310 [cited in previous office action].

5. As to claims 1, 9, and 18, Thor teaches an intelligent clock generating system and method to provide the core clock with at least one clock signal of plurality of clock signals to be used as the core clock signal, wherein plurality of clock signals includes a master clock [first clock with a first frequency] and at least one ramped clock signal

[second clock is generated with a pluralities of clock frequencies] and provides the core clock having a frequency which provides for gradually increasing in a substantially linear or ramped fashion during transition from idle state to the active state [linear increase in frequency inherently having a beginning frequency at start, an intermediate frequency, and end frequency when it reaches the active state][abstract, col. 4, lines 26 – 33, col. 5, lines 9 – 40, col. 6, lines 55 - 59].

However, Thor' s intelligent clock generating system with linear transitioning does not disclose clock frequency generation by dropping selected pulses of clock over a period of time.

Denise discloses a pulse generator and method of controlling outputting frequency with a selection of multiple frequency reduction from source frequency [first clock] in a linear fashion as described in formula [linear relationship] by suppressing selected number of pulses from the output in the predetermined time interval [over a period of time] including a reference clock generator [Oscillator] configured to generate a reference clock signal [col. 2, lines 54 – 56]; and method for generating a plurality of clock frequencies over a period of time [predetermined time interval] in a linear manner [col. 1, lines 47 – 67, col. 2, lines 1 – 67, col. 3, lines 1 – 40, fig. 1].

It would have been obvious to one of ordinary skill in art, having the teachings of Thor and Yenisey before him at the time of invention was made, to modify intelligent clock generating as disclosed by Thor to include a outputting a frequency by suppressing a selected number of pulses available in predetermined time interval as taught by Yenisey in order to obtain output with minimize the variations in the interval of

consecutive output pulses caused by omitted pulses with selected binary weighted sets to produce the desired number of output pulses in a specified period [col. 2, lines 31 – 37] and moreover the combination will provide both to increase or decrease the frequency.

6. As to claims 2, 10, and 19, Thor discloses to select a sequence of values from a storage element [260, shift register] utilizing a first clock [col.7, lines 37 - 46, col. 8, lines 12 – 21].

7. As to claims 3, 11, and 20, Thor discloses a first shift register [260] and second shift register [282] and alternate selection of sequence of values [col. 7, lines 37 – 67,col. 8, lines 22 – 33, col. 9, lines 30 – 38, col. 12, lines 8 – 19, 43 – 67].

8. As to claims 4, 12, and 21, Yenisey discloses a suppressing [dropping] selected number of pulses in performing transition [reducing frequency] inherently include dropping [suppressing] successively greater or fewer number of pulses [col. 2, lines 21 – 37, col. 3, lines 14 – 29, col. 4, lines 11 – 24].

9. As to claims 6, 14, and 23 Thor teaches loading [storing] a shift register [260] with predetermined [desired] values [length of time][col. 7, lines 37 – 39].

10. As to claims 7, 15, and 23, Thor teaches changing a contents of said shift registers at selected times [idle to active state transition] in order to generate second clock [core clock] with an increasing frequency [col. 5, lines 23 – 45, col. 6, lines 65 – 67, col. 7, lines 25 – 46, col. 9, lines 30 – 38, col. 12, lines 10 – 13, 42 – 67, col. 13, lines 1 - 7].

11. As to claims 8, 16, and 24, Thor teaches changing a contents of said shift registers at selected times [enters into idle state] in order to generate second clock [core clock] with an decreasing frequency [col. 8, lines 7 – 21, col. 13, lines 35 - 40].

12. As to claim 17, Thor teaches an intelligent clock generator circuit included within processor [microprocessor][col.3, lines 7 – 13, col. 4, lines 18 - 33].

13. As to claim 25, Thor teaches a system controller coupled to processor and coupled to receive reference clock signal [fig. 1, 3].

14. As to claim 26, Thor's system discloses a screen saver [col. 8, lines7 – 9] with controller and power management, which inherently teach controller coupled to a main memory, graphic adapter, and peripheral bus controller.

15. **Examiner's note**: Examiner has cited particular columns and line numbers in the references as applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings of the art and are applied to the specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant in preparing responses, to fully consider the references in entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the Examiner.

16. **Prior Art not relied upon**: Please refer to the references listed in attached PTO-892, which, are not relied upon for claim rejection since these references are relevant to the claimed invention.

Response to Arguments

17. Applicant's arguments with respect to claims 1 – 26 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin C. Patel whose telephone number is 571-272-3675. The examiner can normally be reached on 6:45 am - 5:15 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne H. Browne can be reached on 571-272-3670. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Nitin C. Patel
May 18, 2005

LYNNE H. BROWNE
SUPERVISORY PATENT EXAMINER
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